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EXAMINER	
CORRIELUS, JEAN B	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/786,670	EICHRODT ET AL.	
	Examiner	Art Unit	
	Jean B. Corrielus	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-27,29 and 31-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-19,21,26,27,29 and 31-38* is/are rejected.

7)☒ Claim(s) *20, 22-25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 19-21, 26, 27, 29, 31 and 35 are objected to because of the following informalities: claim 19, the first monostable circuit does not include any signal input and the claim does not recite how such a circuit is connected to the previous circuit component(s), recited in the claim(s). The second monostable circuit does not include any signal output . Claim 19, the current mirror does not include any signal input and the claim does not recite how such a circuit is connected to the previous circuit component(s), recited in the claim(s). the resistor-capacitor circuit does not include any signal output. As per claim 21, the comparator does not include any signal input and the claim does not recite how such a circuit is connected to the previous circuit component(s) and the limitation “a maximum value counter” has no signal output. As per claim 26, the “means for monitoring” is disclosed to correspond to the structure 203 shown in fig. 7 and “means for generating” is disclosed to correspond to the structure 205 shown in fig. 7. The structure 203 "means for monitoring” however is not seen to include a “signal integrity supervisor”, as presently claim. Both 203 "means for monitoring" and 205 "means for generating” are disclosed to form part of a signal integrity supervisor, per fig. 7. As per claim 35, the “delta sigma modulator” does not include any signal input and output. Any claim whose base claim is objected is likewise objected. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. Applicant's comment has overcome the outstanding 112 rejection of claim 35.

3. Applicant's response has overcome the 112 second paragraph rejection of claims 19-25 and 32.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 32 is rejected under 35 U.S.C. 102(b) as being anticipated by Kawasugi Seiichi Japanese Patent No. JP356143739A.

As per claim 32, Kawasugi Seiichi teaches a transmission circuit fig. 2 comprising: and A/D converter and a gate circuit 17 considered as the claimed "signal integrity supervisor" configured to generate a response (output of circuit 17) to a digital data stream having an anomalous condition see inputs to circuit 17 the gate circuit 17 (signal integrity supervisor) configured to forward the response to circuit 13 considered as the claimed " control logic" capable of resetting the transmission circuit 10 (note that, in response to the anomalous signal, a string of signals is sent to circuit 13, the string of zeros is by definition a reset signal) (see abstract).

6. Claim 26 is rejected under 35 U.S.C. 102(b) as being anticipated by Hatata et al US Patent No. 4,481,629.

Hatata et al teaches a circuit comprising means 2 for monitoring a digital data stream (output of circuit 1) , wherein the means for monitoring a digital data stream

comprises a consistency detecting circuit 4 (signal integrity supervisor); and Hatata includes a inherently a means for generating an output signal 4a (because in order to generate an output signal 4a, a means for generating such a signal has to be provided) in response to an anomalous condition in the digital data stream, wherein the means for generating an output signal is responsive to a digital data stream having a number of consecutive data values of equal magnitude wherein the number of consecutive data values reaches a predetermined maximum value (3 consecutive data values) (see abstract and col. 2, lines 10-18.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawasugi Seiichi Japanese Patent No. JP356143739A in view of Buer US Patent No. 6,188,257.

As per claim 33, as applied to claim 32 above, Kawasugi Seiichi teaches every feature of the claimed invention but does not explicitly teach the additional limitation of "wherein the digital data stream anomalous condition is a clock signal frequency that falls below a predetermined minimum value". Buer teaches the additional limitations of "the digital data stream anomalous condition is a clock signal frequency that falls below a predetermined minimum value". See col. 1, line 65-col. 2, line 2.

Given that fact, it would have been obvious to one skill in the art to incorporate such a teaching in Kawasugi Seiichi so as to minimize signal processing error since the system would have been allowed to act on abnormal signal.

9. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawasugi Seiichi Japanese Patent No. JP356143739A.

As per claim 34, as applied to claim 32 above, Kawasugi Seiichi teaches every feature of the claimed invention but does not explicitly teach the additional limitation the digital data stream anomalous condition is a data signal having a corresponding data value that does not vary for a predetermined maximum number of clock cycles. However, it would have been obvious to one skill in the art to configure Kawasugi Seiichi in such a way as set the anomalous condition as at a data signal having a corresponding data value that does not vary for a predetermined maximum number of clock cycles so as to provide proper means to identify signal abnormalities so as to provide proper compensation.

10. Claims 15, 16, 19, 37 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawasugi Seiichi Japanese Patent No. JP356143739A in view of Nakatani US Patent No. 6,130,619.

As per claim 15, Kawasugi Seiichi teaches a transmission circuit fig. 2 comprising: and A/D converter and a gate circuit 17 considered as the claimed “signal integrity supervisor” configured to generate a response (output of circuit 17) to a digital data stream having an anomalous condition see inputs to circuit 17 the gate circuit 17

(signal integrity supervisor) configured to forward the response to circuit 13 considered as the claimed "line driver" within the AFE (fig. 2, 10). (See abstract).

However, Kawasugi Seiichi does not teach "a clock detector configured to receive a clock signal input and generate a first output signal in response to an at least one clock signal input anomalous condition, wherein the clock detector is further configured to forward the first output signal to at least one of control logic." Nakatani teaches "a clock detector (30 and 40) configured to receive a clock signal input from clock generator 10 and generate a first output signal (see output of circuit 40) in response to an at least one clock signal input anomalous condition (see output of circuit 30), wherein the clock detector (30 and 40) is further configured to forward the first output signal to circuit 20 (at least one of control logic) that includes a microprocessor. It would have been obvious to one skill in the art to incorporate such a teaching in Kawasugi Seiichi in order to determine abnormal conditions related to a clock signal in a communication device as to provide proper compensation.

As per claim 16, Kawasugi Seiichi and Nakatani teach every feature of the claimed invention but do not explicitly teach the first output is a reset signal. However, it is well known in the art to use a clock detector to generate a reset signal. Given that, it would have been obvious to one skill in the art to configure Kawasugi Seiichi clock detector in such a way as to output a reset signal in order to ensure proper operation of the transmission apparatus. Since the apparatus would have been reset to a predetermined desired state that would have enhanced signal processing.

As per claim 19, Kawasugi Seiichi and Nakatani teach every feature of the claimed invention but do not explicitly teach the clock detector includes first and second monostable circuits. Note however that it is well known in the art to incorporate monostable circuits in clock detector as monostable circuits behave well with other circuit components and are also easy to implement.

As per claim 37, see the rejection of claim 15.

As per claim 38, Kawasugi Seiichi teaches a transmission circuit fig. 2 comprising: and A/D converter and a gate circuit 17 considered as the claimed “signal integrity supervisor” configured to generate a response (output of circuit 17) to a digital data stream having an anomalous condition see inputs to circuit 17 the gate circuit 17 (signal integrity supervisor) configured to forward the response to circuit 13 considered as the claimed “ control logic” capable of resetting the transmission circuit 10 (note that, in response to the anomalous signal, a string of signals is sent to circuit 13, the string of zeros is by definition a reset signal) (see abstract).

11. Claim 17 is rejected under 35 U.S.C. 10.3(a) as being unpatentable over Kawasugi Seiichi Japanese Patent No. JP356143739A in view of in view of Nakatani US Patent No. 6,130,619 and further in view of Cummiskey US Patent No. 4,353,128.

As applied to claim 15 above, Kawasugi Seiichi and Nakatani teach every feature of the claimed invention but do not explicitly teach the further limitation that a power down signal is generated in response to the data signal having an unchanging value. Cummiskey teaches the generation of "shut down signal" (power down signal) in response to the data signal having an unchanging value see col. 15, lines 39-41. It

would have been obvious to one skill in the art to modify Kawasugi Seiichi and Nakatani by turning off the power when a data signal having an unchanging value is received as suggested by Cummiskey so as to prevent the system from processing invalid data signal and at the same time to minimize power consumption and to increase battery life.

12. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawasugi Seiichi Japanese Patent No. JP356143739A in view of Nakatani US Patent No. 6,130,619 and further in view of Kodra US patent No. 6,226,663.

As applied to claim 15 above, Kawasugi Seiichi and Nakatani teach every feature of the claimed invention but do not explicitly teach the further limitation of a sigma delta modulator configured to provide the data signal. Kodra teaches a sigma delta modulator 12 configured to provide the data signal to monitor 22. Given that fact, it would have been obvious to one skill in the art to use a sigma delta modulator to produce the data signal so as to take advantage of the inherent property of the sigma delta modulator which makes the probability of encountering a long string of consecutive ones or zeroes during nominal operation to be very small.

13. Claim 21 is rejected under 35 U.S.C. 10.3(a) as being unpatentable over Kawasugi Seiichi Japanese Patent No. JP356143739A in view of Nakatani US Patent No. 6,130,619 and further in view of Kamoi et al US patent No. 5,280,483.

As applied to claim 15 above, Kawasugi Seiichi and Nakatani teach every feature of the claimed invention but do not explicitly teach the further limitation the data supervisor comprising a comparator and a maximum number counter. Kamoi et al

teaches a measuring unit 256 (data supervisor) comprising a comparator 283 and a maximum value (number) counter 281. Given that fact, it would have been obvious to one skill in the art to incorporate such a teaching in Kawasugi Seiichi and Nakatani so as to allow the system to detect accurately signal errors from the input signal.

14. Claims 35 and 36 are rejected under 35 U.S.C. 10.3(a) as being unpatentable over Kawasugi Seiichi Japanese Patent No. JP356143739A in view of Nakatani US Patent No. 6,130,619 and further in view of Hollenbach et al US patent no. 6,396,877.

As per claim 35, as applied to claim 15 above, Kawasugi Seiichi and Nakatani teach every feature of the claimed invention but do not explicitly teach the further limitation of a sigma delta modulator coupled to the clock detector and data supervisor. Hollenbach et al teaches a sigma delta modulator see for instance 200 of fig. 2 to the clock detector (312, 314, 316, 318, 320) and data supervisor (322). Given that fact, it would have been obvious to one skill in the art to incorporate such a teaching in Kawasugi Seiichi in order to take advantage of the inherent property of the sigma delta modulator which makes the probability of encountering a long string of consecutive ones or zeroes during nominal operation to be very small.

As per claim 36, Hollenbach teaches that the sigma delta modulator includes an A/D converter see col. 3, lines 35-45. Given that fact it would have been obvious to one skill in the art to configure the sigma delta to include an A/D so as to be able to convert analog signal into resultant digital signal so as to provide compatibility to system that uses digital signal processors that require a digital signal as input.

15. Claim 27 is rejected under 35 U.S.C. 10.3(a) as being unpatentable Hatata et al US Patent No. 4,481,629 in view of Bartelink US patent No. 4,390,750.

As applied to claim 26 above, Hatata et al teaches every feature of the claimed invention but does no teach the limitations of the anomalous condition would create a DC signal. As evidence by Bartelink, it is known for an anomalous condition to create a DC signal. Given that, it would have been obvious to one skill in the art to modify Hatata et al in such a way to create a DC signal during an anomalous condition in order to provide proper compensation for DC offset so as to improve data detection.

16. Claim 29 is rejected under 35 U.S.C. 10.3(a) as being unpatentable Hatata et al US Patent No. 4,481,629 in view of Nakatani US Patent No. 6,130,619.

As applied to claim 26 above, Hatata et al teaches every feature of the claimed invention and further teaches that the signal integrity supervisor includes a data supervisor and does no teach the limitations of a clock detector included in the signal integrity supervisor. Nakatani teaches “a clock detector (30 and 40) configured to receive a clock signal input from clock generator 10 and generate a first output signal (see output of circuit 40). It would have been obvious to one skill in the art to incorporate such a teaching in Hatata in order to determine abnormal conditions related to a clock signal in a communication device as to provide proper compensation.

17. Claim 31 is rejected under 35 U.S.C. 10.3(a) as being unpatentable Hatata et al US Patent No. 4,481,629 in view of Buer US Patent No. 6,188,257.

As per claim 31, Hatata teaches every feature of the claimed invention but does not explicitly teach the means for generating an output signal is responsive to a digital data stream having a clock signal that falls below a predetermined minimum frequency. Buer teaches a method and apparatus comprising a circuit fig. 1 to generate a response "reset" to a digital data stream (note that the signal on lines 151 and 152 have to be a digital signal since such signal is provided to a digital circuit) having an anomalous condition i.e. a clock signal frequency that falls below a predetermined minimum value. See col. 1, line 65- col. 2, line 2. Given that fact, it would have been obvious to one skill in the art to incorporate such a teaching in Hatata so as to minimize signal processing error since the system would have been allowed to act on abnormal signal.

Allowable Subject Matter

18. Claims 20 and 22-25 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Response to Arguments

19. Applicant's arguments with respect to claims 32-34 have been considered but are moot in view of the new ground(s) of rejection. Applicant stated that fig. 4A and fig. 4B and corresponding text correspond to the means plus function limitations as recited in claim 26. Such point of argument is not convincing, because claim 26 recites "means for monitoring" includes a signal integrity supervisor shown in fig. 4 (A and B) as element 80. Accordingly, the structure corresponding to the **means for generating** would be missing, as the means of monitoring are claimed independently from the means for

generating. As noted above, it appears the corresponding structures of the means plus function limitations recited in claim 26 are incorporated in fig. 7 rather(see comment made above under claim objection). Applicant argues that Kawasugi fails to disclose or even suggest "a line driver within the transmission unit, wherein the response powers down the line driver", as recited in claim 32. However, it is noted that such limitation does not require to be present in Kawasugi to meet the claim limitations because of the recitation "**at least one**" in claim 32, line 4. s argument with respect to claim objection to claim 15 has been withdrawn because the clock detector and the data supervisor are disclosed to be independent from each other as shown in fig. 4B. applicant further argues that Hatata does not teach or even suggest a digital data stream having a number of consecutive values of equal magnitude, as recited in claim 26. However, it is noted that Hatata, teaches, see abstract, last two lines, the consecutive digital sampled **are the same.** Because Hatata discloses that the digital signals are **the same**, they have to have **the same magnitude**. Hence, such limitation is taught by Hatata. Applicant alleges that Kawasugi discloses circuit 13 as "transmitting circuit" which is completely different than "a line driver". However, under the broadest reasonable interpretation, "the transmitting circuit" 13 of Kawasugi can be a line driver, because both the "line driver" and the "transmitting circuit" 13 are configured to transmit a received signal.

Conclusion

20. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean B. Corrielus whose telephone number is 571-272-3020. The examiner can normally be reached on Monday-Thursday from 9:30-3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jean B Corrielus/
Primary Examiner
Art Unit 2611